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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/716,984	11/18/2003	Kevin Raymond Driscoll	13358.0010USC1	6826	
7:	590 05/19/2006		EXAMINER		
MATTHEW LUXTON, ESP.			MASKULINSKI, MICHAEL C		
HONEY WELL 2600 RIDGWA	, INTERNATIONAL , I Y PARKWAY	ART UNIT	PAPER NUMBER		
MINNEAPOLIS, MN 55413			2113	<u>-</u>	
			DATE MAILED: 05/19/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

			Application No.	Applicant(s)			
Office Action Summary			10/716,984	DRISCOLL, KEVIN RAYMOND			
			Examiner	Art Unit			
		1	Michael C. Maskulinski	2113			
Period fo	The MAILING DATE of this commun or Reply	ication appe	ars on the cover sheet with the	correspondence ad	ldress		
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FO CHEVER IS LONGER, FROM THE M nsions of time may be available under the provisions SIX (6) MONTHS from the mailing date of this comm of period for reply is specified above, the maximum sta- re to reply within the set or extended period for reply reply received by the Office later than three months a end patent term adjustment. See 37 CFR 1.704(b).	AILING DAT of 37 CFR 1.136 junication. atutory period will will, by statute, ca	TE OF THIS COMMUNICATIO (a). In no event, however, may a reply be ti apply and will expire SIX (6) MONTHS from ause the application to become ABANDONI	N. mely filed n the mailing date of this c ED (35 U.S.C. § 133).			
Status							
1) 又	Responsive to communication(s) file	d on <i>02 Ma</i> y	v 2006.				
,	This action is FINAL . 2b) ☐ This action is non-final.						
•	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
,	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims						
4)🖂	4) Claim(s) <u>1-26</u> is/are pending in the application.						
•	4a) Of the above claim(s) is/are withdrawn from consideration.						
5)	Claim(s) is/are allowed.						
6)⊠	☐ Claim(s) <u>1,10,12-14,23,25 and 26</u> is/are rejected.						
·	Claim(s) <u>2-6,9,11,15-19,22 and 24</u> is/are objected to.						
8)	Claim(s) are subject to restric	tion and/or	election requirement.				
Applicati	on Papers						
9)	The specification is objected to by the	e Examiner.	•				
,—	•		oted or b) objected to by the	Examiner.			
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including				FR 1.121(d).		
11)	The oath or declaration is objected to						
Priority ι	ınder 35 U.S.C. § 119						
· ·	Acknowledgment is made of a claim	for foreign p	riority under 35 U.S.C. § 119(a	n)-(d) or (f).			
a)	☐ All b)☐ Some * c)☐ None of:			•			
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority				01.		
	3. Copies of the certified copies			ed in this National	Stage		
	application from the Internatio		• • • • • • • • • • • • • • • • • • • •	1			
* 8	See the attached detailed Office action	n for a list of	the certified copies not receiv	ea.			
Attachmen			_				
	e of References Cited (PTO-892)	TO 046'	4)				
	e of Draftsperson's Patent Drawing Review (P mation Disclosure Statement(s) (PTO-1449 or		5) Notice of Informal		O-152)		
	r No(s)/Mail Date <u>5/2/06</u> .	,	6) 🗌 Other:				

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Final Office Action

Double Patenting

In view of the terminal disclaimer filed, the rejection of claims 1-6, 9-19, and 22-26 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5, 8-12, 14-18, 20-24 of U.S. Patent No. 6,678,836 B2, the rejection has been withdrawn.

Claim Rejections - 35 USC § 102

- 1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 2. Claims 1, 10, 13, 14, 23, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Doucer, U.S. Patent 5,838,893.

Referring to claims 1 and 14:

- a. In column 2, line 67 continued in column 3, lines 1-3, Doucer discloses that the system generates a remapping value that when applied to the addresses in the range remaps the range of bad addresses to the highest possible addresses (generating a remapping value).
- b. In column 3, lines 3-6, Doucer discloses that when the system receives an address to use in accessing memory, the system generates a remapped address by applying the remapping value to the received address (logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the remapping value is logically combined with only intended address

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values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values).

c. In column 3, lines 6-7, Doucer discloses that the system then accesses memory using the remapped address (accessing a memory location having the remapped address value).

Referring to claims 10 and 23, in column 3, lines 24-27, Doucer discloses that the system applies the remapping value to the received address by performing a bitwise exclusive-OR of the bits of the received address with the bits of the remapping value (wherein the remapping value and the intended address value are exclusively-Ored to produce the remapped address value).

Referring to claims 13 and 26, in column 4, lines 63-65, Doucer discloses that the remapping value is stored in a register. A register inherently is made of at least one latch, therefore, Doucer teaches latching the remapping value.

Claim Rejections - 35 USC § 103

- 3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 4. Claims 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doucer, U.S. Patent 5,838,893 as applied to claims 1 and 14 above, and further in view of Logic and Computer Design, by Mano et al.

Referring to claims 12 and 25, in column 3, lines 24-27, Doucer discloses that the system applies the remapping value to the received address by performing a bitwise

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exclusive-OR of the bits of the received address with the bits of the remapping value. However, Doucer doesn't explicitly disclose using an exclusive-NOR to reproduce the remapping address value. On page 75, Mano et al. disclose that the exclusive-NOR is the complement of the exclusive-OR. It would have been obvious to one of ordinary skill at the time of the invention to include the exclusive-NOR of Mano et al. into the system of Doucer. A person of ordinary skill in the art would have been motivated to make the modification because an XOR and XNOR gate can be used interchangeably since one is just the complement of the other (see Mano et al.: page 78). Therefore, it is a matter of design choice as to which one is used.

Allowable Subject Matter

5. Claims 2-6, 9, 11, 15-19, 22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

- 6. Applicant's arguments filed May 2, 2006 have been fully considered but they are not persuasive.
- 7. On page 5, under the section, <u>Claims 1, 10, and 13</u>, the Applicant argues, "Douceur re-maps *all* (emphasis by Applicant) addresses rather than remapping only the bad addresses." Further, on page 6, the Applicant argues, "When viewed in isolation, Applicant can understand why the Examiner was confused in stating that '[t]he

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Examiner could not find in the specification where page 0 and 10 are good pages.' However, when reading the example as a whole and viewing Figs. 3, 4, and 5 of Douceur together, it is clear that Douceur illustrates application of the remapping value to all 15 pages. It is true that Douceur did not explicitly say that pages 0-4 and 6-15 were good; however, Applicant respectfully asserts that it is inherent from the totality of the example that these pages are good. If Applicant is to take the Examiner's assumption from Fig. 5 of Douceur that remapping is applied only (emphasis by Applicant) to bad memory locations, the Applicant would have to conclude all (emphasis by Applicant) memory locations are bad because Fig. 4 of Douceur shows the remapping value applied to all (emphasis by Applicant) pages of the memory." The Examiner respectfully disagrees. Although, the Applicant makes some interesting conclusions based on assumptions made about Douceur, the Applicant is incorrect. Why would Douceur specifically state in column 2, lines 62-64, The present invention provides a method and system for remapping memory addresses that address bad memory locations if Douceur intended to remap all addresses? Further, why would Douceur specifically state in column 3, lines 58-65, The remapping system scans physical memory to determine which memory locations are bad. The system then identifies the lowest address and the highest address of the memory locations that are bad. The system then generates a remapping value that will remap this range of memory locations to the highest physical memory range if Douceur intended to remap all addresses? In fact having a range of addresses would be a valid reason as to why it appears Figure 4 is remapping all addresses, when it is only a section of memory that is

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bad. For these reasons it is clear that Douceur does not remap all addresses as stated by the Applicant. The Examiner requests that the Applicant withdraw this argument.

- 8. On page 8, under the section <u>Claims 14, 23, and 26</u>, the Applicant argues, "Douceur does not teach pr suggest remapping *only* (emphasis by Applicant) addresses associated with bad memory address values." The Examiner respectfully disagrees for at least the reasons given in paragraph 7 above.
- 9. On pages 9-10,under the section <u>Rejections Under 35 U.S.C. § 103</u>, the Applicant argues, "Applicant respectfully asserts that claim 12 is not obvious in view of the combination of Douceur and Mano et al." The Examiner respectfully disagrees for at least the rejection above.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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